Remarks

In the present response, two claims (1 and 12) are amended. Claims 1-20 are presented for examination.

I. Claim Rejections: 35 USC § 102(e)

Claims 1, 3, 4, and 12-14 are rejected under 35 USC § 102(e) as being anticipated by US 2003/0088608 (McDonald). Applicants respectfully traverse this rejection.

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. See MPEP § 2131, also, *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Since McDonald neither teaches nor suggests each element in the claims, these claims are allowable over McDonald.

McDonald generally describes a common ready queue. In other words, the queue resides in memory accessible to all CPUs. Their queue is addressed at the same virtual location on all CPUs. When these virtual addresses are read, **the same data is presented to each CPU**. Further, McDonald discusses thread specific information, as in FIG. 5. There are attributes in this structure, but they are attributes of the thread, not the CPU or RAD. Further, the thread structure in McDonald is addressed at the same address by all CPUs because it is a common ready queue. Accessing common memory and structures, as in McDonald, slows down the system because of the latency of the NUMA memory.

In contrast to McDonald, one exemplary embodiment of Applicants' invention describes data that are addressed at the same virtual addresses by different CPUs in different RADs. Each CPU in a different RAD sees <u>different</u> data, specific to its RAD. As such, a CPU can quickly determine the attributes of the RAD it is part of.

Claim 1 recites a first functional unit (i.e., a first RAD) that executes a first program referencing a virtual address. Claim 1 then recites a second functional unit (i.e., second RAD) that executes a second program **referencing the same virtual address**. Claim 1 then recites the following:

> wherein the referencing the virtual memory address by the first program provides a pointer to an attribute stored in the RAM of the

first functional unit, and wherein the referencing the virtual memory address by the second program provides a pointer to an attribute stored in the RAM of the second functional unit and the pointer and the attribute of the second functional unit are different than the pointer and attribute of the first functional unit..

McDonald does not teach or even suggest these recitations. In fact, as noted above, McDonald works in a completely different way.

For at least these reasons, independent claim 1 and its dependent claims are allowable over McDonald.

Claim 12 also recites numerous recitations that are not taught or even suggested in McDonald. By way of example, claim 12 recites "addressing data at a same virtual address by different processors in different functional units, wherein each processor in a different functional unit reads different data specific to its functional unit." As noted above, McDonald works in a completely different way.

For at least these reasons, independent claim 12 and its dependent claims are allowable over McDonald.

II. Claim Rejections: 35 USC § 103(a)

Claim 5 is rejected under 35 USC § 103(a) as being unpatentable over McDonald in view of Boyce. This rejection is traversed.

As noted in section I, McDonald does not teach or even suggest all the elements of independent claim 1. Boyce fails to cure the deficiencies of McDonald. Thus, for at least the reasons given in connection with independent claim 1, dependent claim 5 is allowable over McDonald and Boyce.

III. Claim Rejections: 35 USC § 103(a)

Claims 2, 6-11, and 15-20 are rejected under 35 USC § 103(a) as being unpatentable over McDonald in view of USPN 6,092,157 (Suzuki). This rejection is traversed.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143. For at least the following reasons, Applicants assert that the rejection does not satisfy these criteria.

Independent claims 6 and 15 recite numerous recitations that are not taught or suggested in McDonald and Suzuki. By way of example, claim 6 recites two different RADs, each RAD having a RAM. The claim then recites that each RAD has a replicated portion of the operating system stored in the RAM. In other words, each RAD includes a "**replicated portion**" of the operating system in memory. The Office Action argues that McDonald teaches these recitations at paragraph [0043]. Applicants respectfully disagree.

Paragraph [0043] of McDonald discusses FIG. 3. This figure shows the operating system level 302 that is above the hardware level 301. Paragraph [0043] provides a general discussion of functions for the operating system. Nowhere does paragraph [0043] state or even suggest that each RAD has a RAM that includes a "replicated portion" of the operating system. Again, paragraph [0043] in McDonald merely provides an overview of functions that an operating system performs.

For at least these reasons, independent claims 6 and 15 and their dependent claims are allowable over McDonald and Suzuki.

CONCLUSION

In view of the above, Applicants believe that all pending claims are in condition for allowance. Allowance of these claims is respectfully requested.

Any inquiry regarding this Amendment and Response should be directed to Philip S. Lyren at Telephone No. 832-236-5529. In addition, all correspondence should continue to be directed to the following address:

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